REMARKS/ARGUMENTS

Claims 1-11 are pending. Claim 1 has been amended. Reconsideration is respectfully requested.

Claims 1-11 are rejected under 35 U.S.C. §102(b) as being anticipated by *Wong* (U.S. Pat. No. 5,739,567). Applicants respectfully traverse the Examiner's rejections, noting that the cited reference fails to disclose every element of amended claim 1. For example, *Wong* does not disclose forming a conductor on the planar surface wherein the conductor serving as a gate for a transistor between adjacent trenches, or forming a control gate in each trench wherein each control gate is continuous in a first direction parallel to the trench. In addition, *Wong* does not disclose every element of claims 3-5, 8, or 10-11.

Amended claim 1 recites forming a conductor on the planar surface, wherein *the conductor serving as a gate for a transistor between adjacent trenches*. *Wong* discloses methods of manufacturing an array of vertical memory cells wherein polysilicon is deposited on the array to fill a trench and subsequently patterned to form control gates or word lines of the memory cells. (i.e., *Wong*, col. 11, lines 3-10; col. 20, lines 45-48). The control gates or word lines are patterned so that they are perpendicular to the trench. (i.e., *Wong*, Figs. 11, 13, 16, 22, 24). However, *Wong* does not disclose a conductor serving as a gate for a transistor between adjacent trenches. Therefore, Applicants respectfully submit that claim 1 is patentable over the cited reference and in condition for allowance for at least this reason.

Furthermore, amended claim 1 recites forming a plurality of spaced apart trenches in a first direction, and forming a control gate in each trench *wherein each control gate is continuous in the first direction.* As described previously, Wong discloses that the control gates or word lines are patterned so that they are perpendicular to the trench. In other words, *Wong* discloses that forming control gates *that are discontinuous in a direction parallel to the trench.* (i.e.,

Wong, Figs. 11, 13, 16, 22, 24). In contrast, claim 1 requires that each control gate is continuous in the first direction parallel to the trench. Therefore, Applicants respectfully submit that claim 1 is patentable over the cited reference and in condition for allowance for at least this additional reason.

Claims 2-11 depend from claim 1. Applicants respectfully submit that claims 2-11 are therefore patentable over the cited reference for at least the same reasons that claim 1 is patentable over the cited reference. Moreover, claims 3-4, 5, 8, and 10-11 are further patentable over the cited reference for at least the additional following reasons.

Regarding claim 3 and claim 10, *Wong* does not disclose forming a tip along each of the floating gates at an end closest to the bottom wall of the trench. Similarly, regarding claim 4 and claim 11, *Wong* does not disclose forming a tip along each of the floating gates at an end furthest away from said bottom wall in each trench. The Examiner cites *Wong* at col. 10, lines 45-60 as teaching "that the floating gates are etched and would naturally leave somewhat rounded ends and has a tip along the floating gates at an end closest to the bottom of the trench and tip that is further away from the bottom wall." (Office Action dated 08/04/05, pg. 2). However, the section cited by the Examiner discloses depositing a layer of PDO 1032 that is thinner in a trench than on a top surface of an array so that a plasma etch of the PDO exposes the trench without exposing the top of the array. (*Wong*, col. 10, lines 44-51). *Wong* does not disclose that the floating gates are etched and would naturally leave somewhat rounded tips. In fact, *Wong* does not disclose floating gates at all in the passage cited by the Examiner. Applicants' review of *Wong* failed to find any mention of a floating gate having a tip, or that etching the floating gates "would naturally leave somewhat rounded edges". Therefore, Applicants respectfully submit that claims 3-4 and claims 10-11 are patentable over the cited reference and in condition for allowance for at least these additional reasons.

Regarding claim 5, *Wong* does not disclose that the cutting step cuts each pair of floating gates without cutting the control gate. Examiner cites *Wong* at col. 20, lines 47-55 as teaching that the floating gates are etched and the control gates need not be etched. (Office Action dated 08/04/05, pg. 2). However, the section cited by the Examiner expressly states that "floating gates 2305 are self-aligned to control gates 2309 *and are etched in the same etching step as the control gates.*" (*Wong*, col. 20, lines 52-55). Furthermore, Applicants' review of *Wong* failed to find any mention that a cutting step cuts each pair of floating gates without cutting the control gate. Therefore, Applicants respectfully submit that claim 5 is patentable over the cited reference and in condition for allowance for at least this additional reason.

Regarding claim 8, *Wong* does not disclose that the cutting step is performed prior to the control gate being formed in the trench. In contrast, as described previously, *Wong* discloses etching the floating gates in the same step as the control gate, after the control gate is formed in the trench. Therefore, Applicants respectfully submit that claim 8 is patentable over the cited reference and in condition for allowance for at least this additional reason.

For the foregoing reasons, it is respectfully submitted that the claims are in an allowable form, and action to that end is respectfully requested.

If the Examiner feels that a telephone conference would speed prosecution of this application, the Examiner is invited to call Applicants' attorney at the telephone number listed below.

The Commissioner is hereby authorized to charge any fees which may be required or credit any over payment in fees to **Deposit Account No. 07-1896** and reference Attorney Docket **No. 351913-992472**.

Respectfully submitted,

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